REMARKS

Reconsideration of the present application is respectfully requested. No claims have been amended. Claims 44-68 has been canceled. No new claims have been added in this response. No new matter has been added.

Affirmation of Election

Applicant canceled claims 44-68 to affirm the election of claims 1-43.

Claim Rejections

Claim 1 stands rejected under 35 USC §103(a) based on Naffziger et al. (US 6,640,283) and Kever et al. (US 6,735,673). Applicant respectfully traverses the rejections.

As explained in the response to the previous office action mailed on 1/4/2006, the present application discloses a mechanism of compressing two or more cache lines' worth of information into one compressed cache line's worth of information. The compressed cache line's worth of information is then stored back into a program-addressable memory, the system memory of a computing system, for example (as opposed to cache memory that is much faster than the system memory). Thus, rather than requiring two or more system memory accesses to fetch the two or more cache lines' worth of information from, one system memory access is able to fetch the compressed cache line's worth of information and then decompress it into the original two or more cache lines' worth of information. This advantageously reduces the

demand for system memory accesses so as to make the system memory's usage more efficient within the computing system.

Claim 1 recites:

> 1. A memory controller for use in **a system having a program-addressable memory controlled by the memory controller and a processor coupled with the memory by an external bus**, the memory controller comprising a compression map cache to store information that identifies **a compressed cache line's worth of information stored in the memory**, the compressed cache line's worth of information comprising a compressed version of a first cache line's worth of information and a compressed version of a second cache line's worth of information.
> (emphasis added).

By contrast, Naffziger and Kever, individually or in combination, do not teach or suggest the above emphasized limitations.

Zaffziger does not teach or suggest a memory controller controlling a program-addressable memory and comprising a compression map cache to store information that identifies a compressed cache line's worth of information stored in the memory, such as recited in claim 1. The Examiner alleges that Zaffziger teaches a level 2 cache which may be considered as a memory controller such as recited in claim 1 (*see* Final Office Action, page 3). Applicant respectfully disagrees. A level 2 cache is not a memory controller. Even assuming *arguendo* that the level 2 cache of Zaffziger may be considered as a memory controller, the included memory controller is to control the level 2 cache, which is not program-addressable. Although the main memory 110 shown in Zaffziger's Figure 1 is program-addressable, the level 2 cache does not control the main memory 110. Instead, it is the system controller 108 shown in Figure 1 that is controlling the main memory 110 (*see* Zaffziger's column 5, lines 4-8). Zaffziger discloses that the level 2 cache, not the system controller controlling the main memory

110, has a tag memory. Thus, Zaffziger does not teach or suggest each and every limitation of claim 1.

Kever discloses a mechanism of storing compressed data in a cache so that more data may be cached in order to increase the probability of a cache hit (*see* Kever's abstract). The compressed lines of data is stored in a cache, rather than in a program-addressable memory, such as recited in claim 1.

Because Zaffziger and Kever do not teach or suggest the all limitations of claim 1, claim 1 is not anticipated by Zaffziger and Kever.

Independent claims 17, 33, 44 and 57 each recites limitations similar to those discussed above for claim 1. For similar reasons, claims 17, 33, 44, 57 and all claims which depend on them are also patentable over Zaffziger and Kever.

For the foregoing reasons, the present application is believed to be in condition for allowance, and such action is earnestly requested.

If any additional fee is required, please charge Deposit Account No. 02-2666.

Respectfully submitted,
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